

DTIS 2008 Tutorial
Half-day (3 hours, PM)
March 25, 2008

The tutorial will be confirmed if there are at least 10 registered participants.

• Tutorial Title

Power-Aware Testing and Test Strategies for Low Power Devices

• Tutorial fees

The tutorial fees are fixed to 60 Euros (100 TND), which have to be payed in cash at the time of the registration. To register for the DTIS'08 Tutorial, you should send an e-mail to brahim.mezghani@enis.rnu.tn.

• Details of Coordinating Presenter

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• Intended Audience

Test, Design and Design-for-Test practitioners (engineers, engineering managers, students, academics) who are interested in learning more about the impact of power dissipation during manufacturing test, how it is possible to alleviate test power issues, and how low power devices can be tested safely without affecting yield and reliability.

• Tutorial Summary

Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like dynamic voltage scaling, clock gating or power down techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area.

It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

- **Tutorial Program**

1. Introduction
2. Test Power Metrics
 - 2.1 Power Consumption Sources
 - 2.2 Terminology
 - 2.3 Test Power Metrics
3. Test Power Issues
 - 3.1 Overview of Thermal Effects and Noise Phenomena
 - 3.2 Reliability Issues
 - 3.3 Test Throughput Problems
 - 3.4 Manufacturing Yield Loss
4. Test Application Environments
 - 4.1 Slow-Speed Scan Testing
 - 4.2 At-Speed Scan Testing
 - 4.3 Logic BIST
5. Low-Power Test Pattern Based Approaches
 - 5.1 X-Filling Techniques
 - 5.2 Low-Power Test Pattern Generation
 - 5.3 Power-Constrained ATPG
 - 5.4 Low-power Test Vector Compaction
 - 5.5 Low-Power Memory Test Algorithms
6. Low-Power Design-for-Test
 - 6.1 Gated Scan Cells
 - 6.2 Scan Cell Reordering
 - 6.3 Logic Insertion in Scan Chain
 - 6.4 Scan Chain Segmentation
 - 6.5 Staggered Clocking
 - 6.6 Masking Logic Insertion
 - 6.7 Circuit Partitioning
7. Low-Power Test Data Compression
 - 7.1 Coding-Based Schemes
 - 7.2 Linear-Decompression-Based Schemes
 - 7.3 Broadcast-Scan-Based Schemes
8. System-Level Low-Power Testing
 - 8.1 Power-Constrained Test Scheduling
 - 8.2 Power Profile Modification
 - 8.3 Thermal-Aware Test Scheduling
9. Overview of Low Power Design Techniques
 - 9.1 Supply Voltage Scaling
 - 9.2 Adaptive Frequency Scaling
 - 9.3 Gated Clock Architectures
 - 9.4 Power Domain Partitioning
 - 9.5 Test Implications of Low Power Design

10. Test Strategies for Low Power Devices
 - 10.1 Power-Managed Scan Using Adaptive Voltage Scaling
 - 10.2 Test Generation for Multiple Supply Voltage Settings
 - 10.3 Miscellaneous Techniques
11. EDA Tools for Power-Aware Design-for-Test
12. Summary and Conclusions

• **Tutorial Keywords**

Power-aware Testing, Power-Constrained Testing, Low Power Design, Power Management, Test Power Issues, Design-for-Test, Scan Testing, Built-In Self-Test, Test Data Compression, ATPG

• **Proposal book for handout**

Laung-Terng Wang, Charles E. Stroud, and Nur A. Touba, editor, System-on-Chip Test Architectures: Nanometer Design for Testability, Morgan Kaufmann - Elsevier, ISBN: 978-0-12-373973-5, November 2007.

• **Presenters' biographies**

Patrick GIRARD received a M.S. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research), and works in the Microelectronics Department of the LIRMM (Laboratory of Informatics, Robotics and Microelectronics of Montpellier - France). Patrick Girard is the Vice-Chair of the European Test Technology Technical Council (ETTTTC) of the IEEE Computer Society. He is the Editor-in-Chief of the ASP Journal of Low Power Electronics and an Associate Editor of the IEEE Transactions on Computers. He has served as Guest Editor for the Journal of Electronic Testing – Theory and Applications (JETTA) in 2007. He is on the technical program committee of the ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design Automation and Test in Europe (DATE), IEEE International Conference on Computer Design (ICCD), IEEE International Conference on Design & Test of Integrated Systems (DTIS), IEEE VLSI Test Symposium (VTS), IEEE European Test Symposium (ETS), IEEE International On-Line Testing Symposium (IOLTS), IEEE Asian Test Symposium (ATS), ACM/IEEE International Symposium on Low Power Electronic Design (ISLPED), IEEE International Symposium on Electronic Design, Test & Applications (DELTA) and IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS). He has served as Test Track Chair for DAC 2007 and DATE 2007. He has also served as Program vice-Chair for the IFIP International Conference on Embedded And Ubiquitous Computing (EUC) in 2005 and as Program Chair for DELTA 2006, DTIS 2006, and DDECS 2007. He will serve as Program Chair for ETS 2008. Patrick Girard has been involved in numerous European research projects (ESPRIT III ATSEC, EUREKA MEDEA, MEDEA+ ASSOCIATE, IST MARLOW, MEDEA+ NanoTEST) and has managed several industrial research contracts. His research interests include the various aspects of digital testing and memory testing, with special emphasis on DfT, BIST, diagnosis, delay testing, FPGA testing, power-aware testing. He has published 2 books, 30 journal papers, and more than 90 conference and symposium papers on these fields. He received the Best Paper Award at ETS 2004 and at DDECS 2005.

Xiaoqing WEN received a B.E. degree from Tsinghua University, Beijing China, in 1986, a M.E. degree from Hiroshima University, Hiroshima, Japan, in 1990, and a Ph.D degree from

Osaka University, Osaka, Japan, in 1993. From 1993 to 1997, he was a Lecturer at Akita University, Akita, Japan. He was a Visiting Researcher at University of Wisconsin, Madison, U.S.A., from October 1995 to March 1996. He joined SynTest Technologies, Inc., U.S.A., in 1998, and served as its CTO until 2003. In January 2004, he joined the Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. He was the Program Committee Co-Chair of the Sixteenth IEEE Asian Test Symposium and the Eighth IEEE Workshop on RTL and High Level Testing. In addition, he served on the program committees of IEEE Asian Test Symposium (ATS), IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC), IEEE Int'l Symposium on Electronic Design, Test, & Applications (DELTA), IEEE Int'l Conf. on Design & Test of Integrated Systems in Nanoscale Technology (DTIS), IEEE Int'l Test Conference (ITC), IEEE Workshop on RTL and High Level Testing (WRTL), and IEEE Workshop on Defect-Based Testing (DBT). His research interests include low-power test, high-quality test generation, test compression, fault diagnosis, and testable design. He is the Co-Editor of the book "VLSI Test Principles and Architectures: Design for Testability" (Elsevier, 2006), 26 journal papers, and 45 conference and symposium papers. He is a member of the IEEE, the IEICE, and the REAJ.