

Tutorial proposal – DTIS 2006

Title

“Design and validation of dependable integrated systems”

Summary:

Integrated embedded systems are increasingly used in many applications, including critical ones. Such systems are made of specific hardware blocks as well as processor cores running software programs. They can be implemented either in complex FPGAs (System on Programmable Components – SoPCs) or using up-to-date ASIC technologies. In both cases, the probability of transient faults becomes high enough to be seriously accounted for during the system design.

The tutorial will first present a quick overview of on-line threats (fault origins and models) and of the general design approaches used to increase dependability. Then the presentation will mainly focus on two aspects: specific problems and solutions related to SRAM-based FPGAs and multi-level dependable design involving both software and hardware (in particular RTL) techniques. The last part of the tutorial will cover the dependability evaluation and fault injection techniques, again with a special focus on SRAM-based FPGAs. Various examples will be detailed during the tutorial presentation. Practical design constraints in up-to-date design flows will also be addressed.

Keywords:

Integrated systems, dependability, soft errors, FPGA, SoPC, on-line test, fault tolerance, fault injection

Intended public:

Integrated circuit and system designers, both from industry and academia.
Researchers and engineers interested in architecture, FPGA-based design and dependability.

Presenter:

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Short Biography:

Régis LEVEUGLE received the PhD degree in Microelectronics from the National Polytechnical Institute of Grenoble (INPG), France, in 1990. He is currently Professor at this institute and member of TIMA laboratory. His main interests are computer architecture, VLSI design methods and CAD tools, dependability evaluation, fault-tolerant architectures and concurrent checking. He has authored or co-authored more than 100 scientific papers and served as a reviewer for many journals and conferences. He has also served on more than 50 program and organization committees. He was Program co-Chair for the 2001 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'01), vice-General Chair for the 2002 IEEE International On-Line Testing Workshop (IOLT'02), General co-Chair for DFT'02, vice-Program Chair for the 2003 and 2005 IEEE International On-Line Testing Symposium (IOLTS'03 and IOLTS'05) and Program co-Chair for IOLTS'03 and IOLTS'06. He is a member of IEEE.