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Welcome to the IEEE DTIS'06 Conference

Welcome to the 1st edition of the IEEE International Conference on Design & Test of Integrated Systems in Nanoscale Technology, IEEE DTIS'06.

The aim of this International Conference is to cope with the rapidly progressing electronic technology which, today, reaches the nanometer scale. The area of interest for this year's 1st edition of The IEEE DTIS'06 Conference deals with the Design and Test of electronic products, ranging from integrated circuits through multi-chip modules and printed circuit board to full Systems and Microsystems, as well as examining the methodologies and tools used in the design of such products.

The number of submitted papers has been very successful. We received 114 papers from 22 different countries. The three topic areas of these 114 submitted papers are on Design (57%), Test (32%) and Technology (11%). From these 114 submissions, 49 papers have been accepted for oral presentation and an additional 27 papers have been accepted as posters. As a result, a very nice program has been set up including:

- 2 invited keynote speakers on:
 - ✓ Automated Design of Microfluidics-Based Biochips: Connecting Biochemistry to Electronics CAD, which will be given by Dr. Krishnendu Chakrabarty from Duke University, USA.
 - ✓ SiP Technologies: Perspectives and Challenges, which will be given by Dr. Philippe Cauvet from Philips, France.
- 49 oral presentations distributed in two parallel tracks,
- 27 poster presentations distributed in 4 poster sessions,
- 2 special sessions with 4 papers each on:
 - ✓ Software Radio, chaired by Dr. Yann Deval from IXL Laboratory, France and Dr. Chiheb Rebai from SUPCOM Tunis, Tunisia.
 - ✓ Emerging devices: simulation of CNTFET-based circuits, chaired by Dr. Regis Leveugle from TIMA Laboratory, France.
- A tutorial program, chaired by Dr. Regis Leveugle, an important element in our conference, which includes those topic areas that are of great current interest to integrated circuit and system designers, both from industry and academia; and to researchers and engineers interested in architecture, FPGA-based design and dependability. This tutorial will mainly focus on two aspects: specific problems and solutions related to SRAM-based FPGAs and multi-level dependable design involving both software and hardware (in particular RTL) techniques.
- A Forum, chaired by Dr. Lotfi Ben Ammar and Dr. Laroussi Bouzaida, organized by two international companies, ATMEL and ST Microelectronics. This Forum is entitled "Test and Industrialization of nowadays SoCs: Orientations and challenges".

We hope the attendees will enjoy the technical program as well as the social aspect of the conference in the beautiful city of Tunis, in the Gammarth region. It offers proximity to the antique sites of Carthage, the picturesque Village of Sidi Bou Said and La Marsa region. The

Gammarth region is considered to be one of the most beautiful sea side in Tunisia with its charming beaches and nice white houses that lie among the green trees.

The conference chairs would like to thank all of you: the authors who have submitted their research papers and the members of the program committee who have been working hard on the paper reviews. This conference is finally the result of a team effort from voluntary people who have willingly given their time and energy: the Organization Committee who have handled the overall coordination; the Technical Program Committee who made the reviews, and last but by no means least, the MSc and PhD students who gave their valuable help in every organizing step.

We look forward to meet you in Tunisia during the IEEE DTIS'06 Conference and we hope that you will enjoy your stay.

Dr. M. Masmoudi & Dr. M. Renovell
General co-Chairs
IEEE DTIS'06

Dr. P. Girard & Dr. J. Mouine
Program co-Chairs
IEEE DTIS'06

