

IEEE DTIS'06 Final Program

September 5th, 2006

09:00-10:15 OPENING SESSION

09:00-9:15 Welcome Address

M. Masmoudi - ENIS – Tunisia / *M. Renovell* – LIRMM – France
IEEE DTIS'06 General co-Chairs

09:15-09:30 Technical Program Introduction

P. Girard – LIRMM - France / *J. Mouine* – ENIT – Tunisia
IEEE DTIS'06 Program co-Chairs

09:30-10:00 Keynote Address 1

Automated Design of Microfluidics-Based Biochips: Connecting Biochemistry to Electronics CAD; *K. Chakrabarty* – Duke University - USA

10:00-10:15 Official Welcome Message

Minister of Higher Education – Tunisia

10:15-11:15 BREAK & POSTERS

10:15-11:15 Poster Session 1

- **A non-volatile Flip-Flop in Magnetic FPGA chip;** *W.Zhao, E. Belhaire, V. Javerliac, C. Chappert, B. Dieny;* Université Paris Sud, CNRS,-France; SPINTEC, CEA , France.
- **MDCT IP Core Generator;** *M. Baláž, P. Malík, T. Pikula, M. Šimlaští;* Slovak Academy of Sciences Bratislava, Slovakia.
- **Hardware Design and Implementation of Digital Controller for Parallel Active Filters;** *S. Ben Othman, A. Brahem, S.Ben Saoud;* INSAT / LECAP-EPT-Tunisia.
- **Dependability Analysis: Performance Evaluation of Environment Configurations;** *P. Vanhauwaert, R. Leveugle, P. Roche;* TIMA, France; STMicroelectronics, France.
- **Performances evaluation and enhancement of MPEG4 transmission over IEEE 802.11 WLAN;** *N. Moussa, A. Soudani, R. Tourki;* Electronic and Micro-Electronic laboratory, Tunisia.
- **New generic GALS NoC Architectures with Multiple QoS;** *M. Zid, A. Zitouni, A. Baganne, R. Tourki;* Electronic and Micro-Electronic laboratory, Tunisia; Laboratoire Electronique des Systèmes Temps Réel, France.

11:15-12:30 SESSION 1

11:15-12:30 Session 1A: Analog Circuit Design 1

Chair: J. MACHADO DA SILVA - INESC Porto - Portugal

- **Analysis of Timing Jitter in Inverters Induced by Power-Supply Noise;** *A. Strak, H. Tenhunen*; School of Information and Communication Technology KTH - Royal Institute of Technology Stockholm, Sweden.
- **Dual Band CMOS LNA Design with Current Reuse Topology;** *M. Ben Amor, A. Fakhfakh, H. Mnif, M. Loulou*; LETI –Tunisia.
- **A Low-Power Design Methodology for Single-Stage Operational Amplifiers;** *H. Aminzadeh, M. Danaie, R. Lotfi*; Ferdowsi University of Mashhad, Iran.

11:15-12:30 Session 1B: Device Modelling

Chair: B. REZIG – ENIT - Tunisia

- **Speeding up simulation time in EEPROM memory designs;** *H. Aziza, B. Delsuc, J.M. Portal, D. Nee*; L2MP-Polytech Marseille, France; STMicroelectronics, France.
- **Modeling of Pixel Sensors for Image Systems with VHDL-AMS;** *F. Dadouche, A. Pinna, P. Garda, A. Alexandre*; Université Pierre et Marie Curie, France.
- **Two dimensional model for lateral photodiode;** *A. Alexandre, F. Dadouche, P. Garda*; Université Pierre et Marie Curie, France.

12:30-14:00 LUNCH

14:00-15:40 SESSION 2

14:00-15:15 Session 2A: Embedded System Design

Chair: R. TOURKI – FSM - Tunisia

- **Accelerating the Rijndael Algorithm Using Custom Instructions Capability of Nios II in ODYSSEY;** *R. Iraj, S. Hessabi, E. K. Moghadam*; Department of Computer Engineering, Sharif University of Technology, Tehran, Iran
- **Implementation of Scalable Embedded FPGA for SOC;** *H. Mrabet, Z. Marrakchi, H. Mehrez, A. Tissot*; LIP6-ASIM Laboratory; CEA-DAM IDF, France.
- **Method for Embedded Application Prototyping based on SoC Platform and Architecture Model;** *Y. Aoudni, G. Gogniat, K. Loukil, J.L. Philippe, M. Abid*; LESTER- Lorient, France; CES-ENIS, Tunisia.

14:00-15:40 Session 2B: Characterization and Modelling

Chair: J. FIGUERAS – UPC - Spain

- **Additivity of Capacitive and Inductive Coupling in Submicronic Interconnects;** *J.E. Lorival, D. Deschacht, Y. Quere, T. Le Gouguec, F. Huret;* LIRMM, Université de Bretagne Occidentale, France.
- **Ground Bounce Modelling for Digital Gigascale Integrated circuits;** *M. Pons, F. Martorell, X. Aragones, F. Moll, A. Rubio;* Electronic Engineering Department, Universitat Politècnica de Catalunya, Spain.
- **A high-level timing model for variability characterization of interconnect circuits;** *M. Miranda, A. Papanikolaou, H. Wang, M. Kaspiris, P. David, F. Catthoor;* IMEC Belgium, Also Katholieke Universiteit Leuven.
- **SRAM Dedicated PCMs For Leakage Characterization In Nanometer CMOS Technologies;** *S. Leomant, A. Turier, L. Ben Ammar, A. Amara;* ISEP, Paris, France; ATMEL Rousset, France.

15:40-16:40 BREAK & POSTERS

15:40-16:40 Poster Session 2

- **An FPGA Hardware implementation of the Rijndael block cipher;** *C. Dhoha, S. Ben Othman, S. Ben Saoud;* LECAP-EPT / INSAT, Tunisia.
- **Implementation of a fuzzy logic tracking path algorithm on a Field Programmable Gate Array;** *H. Abdelkrim, S. Ben Saoud;* LECAP-EPT / INSAT, Tunisia.
- **Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics;** *N. Badereddine P. Girard S.Pravossoudovitch, C. Landrault, A. Virazel, H.J. Wunderli;* LIRMM, France, Institut für Technische Informatik Universität Stuttgart, Germany.
- **Two-pattern generation based on Accumulators with 1's Complement adders;** *I. Voyiatzis, C. Efstathiou;* Technological Educational Institute of Athens, Greece.
- **High Q-VCO with Low Phase Noise for Communications Applications;** *N. Boughanmi, D. Ben Issa, A. Kachouri, M. Samet;* LETI, Tunisia.
- **Transcutaneous Power And High Data Rate Transmission For Biomedical Implants;** *G. Ben Hmida, M. Dhieb, H. Ghariani, M. Samet;* LETI, Tunisia.
- **Simultaneous Delay optimization and Depth reduction in Logic trees with minimum resources;** *P. Balasubramanian, P. Pasala;* India.

16:40-17:55 SESSION 3

16:40-17:55 Session 3A: Circuit Design Verification

Chair: R. LEVEUGLE – TIMA - France

- **A New Synchronization Policy between PSL Checkers and SystemC designs at Transaction Level;** *Y. Lahbib , M.A Ghrab , M. Hechkel, F. Ghenassia , R. Tourki;* ST Microelectronics, Electronics and Microelectronics Laboratory, Tunisia; ST Microelectronics, France.
- **Physical Verification of Microelectronics “Mask Patterns” with Calibre SVRF Rule Files;** *L. Salager;* STMicroelectronics, France.
- **Verification Flow Optimization using an Automatic Coverage Driven Testing Policy;** *Y. Lahbib , O. Missaoui, M. Hechkel, D. Lahbib , B. Mohamed-Yosri , R. Tourki;* ST Microelectronics, Tunisia; CECS, Louisville, KY, USA; ENSI, Tunisia; Electronic and Micro-Electronic laboratory- Tunisia.

16:40-17:55 Session 3B: Test Trends and SiP Testing

Chair: C. LANDRAULT – LIRMM - France

- **Embedded Flash Testing: Overview and Perspectives;** *O. Ginez , J.-M. Daga P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel ;* LIRMM, France ; ATMEL, France.
- **Trends in Tests and Failure Mechanisms in Deep Sub-Micron Technologies;** *S. Hamdioui, Z. Al-Ars, L. Mhamdi, G. Gaydadjiev, S. Vassiliadis;* Delft University, The Netherlands.
- **Testing System-in-Package wirelessly;** *S. Bernard, D. Andreu, M-L Flottes, P. Cauvet, H. Fleury, F. Verjus;* LIRMM, France ; Philips, France.

September 6th, 2006

08:30-09:45 SESSION 4

08:30-09:45 Session 4A: RF Circuit Design

Chair: M. RENOVELL – LIRMM - France

- **Reliability of Active RF Filters in Nanoscale Region;** *E. Xiao*; Department of Electrical Engineering, University of Texas at Arlington, USA.
- **Design and Optimisation of RF Filters for Multistandard RF Sub-sampling Receiver;** *R.Barrak , A. Ghazel, F. Ghannouchi* ; CIRTA'COM, Tunisia, Intelligent RF Radio Laboratory, Electrical and Computer Engineering Department The University of Calgary, Calgary, Alberta, Canada.
- **Design of Power-controlled Class1 Bluetooth CMOS Power Amplifier;** *A. A. El-sabban, H. F. Ragai*; VLSI Design Center, AOIE, Ain Shams University, Egypt.

08:30-09:45 Session 4B: Innovative Technologies and Synthesis

Chair: L. BEN AMMAR – ATMEL - France

- **Magnetic Domain wall logic requires new synthesis methodologies;** *J.-O. Klein, E. Belhaire, C. Chappert, R. Cowburn, D. Read, D. Petit*; IEF Université Paris Sud, France; Imperial College, Blackett Physics Laboratory, England.
- **Synthesis of Symmetric Functions Using Quantum Cellular Automata;** *Ha_zur Rahaman, Biplab K Sikdar, Debesh K Das*; Bengal Engg and Science University; Jadavpur University, India.
- **Power Aware minimization of Complementary Logic functions based on maximal HD;** *P. Balasubramanian, Y. Sirisha*; School of Electrical Sciences, Vellore Institute of Technology (Deemed University), India.

09:45-10:45 BREAK & POSTERS

09:45-10:45 Poster Session 3

- **Average Modeling of DC-DC and DC-AC converters including Semiconductor Device Non-linearities;** *S. Abid, A. Ammous*; PEG, Tunisia.
- **Behavioral Synthesis Technique for Flexible IP's Communications;** *S. Kamel, I. Bennour, A. Baganne, R. Tourki, A. Jemai*; Electronic and Micro-Electronic laboratory- Tunisia ; L.I.P.2, Tunisia; L.E.S.T.E.R, France.
- **An On-Line Software-Based Self-Test Framework for Microprocessor Core;** *A. Benso, A. Bosio, P. Prinetto, A. Savino*; Politecnico di Torino, Italy.
- **Modulation/Demodulation Techniques With FPGA's Architecture to improve OFDM Wireless Underwater Communication Transceiver;** *N. Nasri, H. Ben Hnia, A. Kachouri, M. Abdellaoui, M. Samet*; LETI, Tunisia.

- **Transaction Level Modeling of an OSI-like Layered NoC;** *S.-H. Sfar, I. Bennour, R. Tourki*; Electronic and Micro-Electronic laboratory, Tunisia.
- **EDP optimized Synthesis scheme for Boolean Read-Once functions;** *P. Balasubramanian, S. Theja*; School of Electrical Sciences, Vellore Institute of Technology (Deemed University), India.
- **Comparison of Addition Structures Synthesis over Commercial FPGAs;** *M.-A. Sacristan, V. Rodellar, A. Diaz*; DATSI, ATC, Spain.

10:45-12:25 SESSION 5

10:45-12:25 Session 5A: Special Session on Software Radio

Chairs: Y. DEVAL – IXL – France; C. REBAI – SUPCOM Tunis - Tunisia

- **Injection Locked Oscillator Based RF Transmitters;** *T. Finateu, J.-B. Begueret, Y. Deval, F. Badets*; STMicroelectronics, France; IXL, France.
- **Low Power FPGA-Based Implementation Of Decimating Filters For Multistandard Receiver;** *N. Khouja, K. Grati, A. Ghazel*; CIRTA'COM Laboratory, SUPCOM, Tunisia.
- **Non-Uniform Sampling Schemes for IF Sampling Radio Receiver;** *M. Ben-Romdhane, C. Rebai, A. Ghazel, P. Desgeys, P. Loumeau*; CIRTA'COM, SPCOM, Tunisia; LTCI-CNRS, France.
- **A Dual-Mode Dual-Standard LNA for DCS1800/W-CDMA Applications;** *C. P. Moreira, E. Kerherve, P. Jarry, D. Belot*; IXL, France; STMicroelectronics, France.

10:45-12:25 Session 5B: Advances in Test and Fault Tolerance

Chair: L. BOUZAIDA – STMicroelectronics - France

- **Mixed-Signal Simulation & Test Generation;** *M. Dufils, J.-L. Carbonero, P. Planelle, P. Raynaud*; STMicroelectronics France; Mentor Graphics, France.
- **Estimation of test metrics for multiple analogue parametric deviations;** *A. Bounceur, S. Mir, E. Simeur, L. Rolіндеzy*; TIMA, France; STMicroelectronics, France.
- **Hybrid fault simulation with compiled and event-driven methods;** *K. Taniguchi, H. Fujii, S. Kajihara, X. Wen*; Department of Computer Science and Electronics Kyushu Institute of Technology, Japan.
- **Defect and Fault Tolerant Cell Architecture for Feasible nanoelectronic designs;** *F. Martorell, A. Rubio*; University Politecnica de Catalunya, Spain.

12:25-14:00 LUNCH

14:00-14:50 SESSION 6

14:00-14:50 Session 6A: Mixed Signal Systems and Hard-Sensor Electronics

Chair: K. CHAKRABARTY – Duke University - USA

- **A novel scalable spiking pixel architecture for deep submicron CMOS technologies;** *F. Boussaid, C. Shoushun, A. Bermak*; University of Western, Australia, Hong Kong University of Science and Technology, Hong Kong.
- **Design and Implementation of An 11-bit Non-linear Interpolation DAC;** *S. Eisa, K. Shehata, H. F. Ragai*; AAST, Ain Shams University, Egypt.

14:00-14:50 Session 6B: Defect and Fault Modelling

Chair: S. HAMDIOUI – Delft University – The Netherlands

- **Analyzing the Memory Effect of Resistive Open in CMOS Random Logic;** *M. Renovell, M. Comte, I. Polian, P. Engelke, B. Becker*; LIRMM, France; Albert-Ludwigs University, Germany.
- **Supply voltage glitches effects on CMOS circuits;** *A. Djellid-Ouar, G. Cathebras, F. Bancel*; LIRMM, France ; STMicroelectronics, France.

15:00-15:30 KEYNOTE 2

SiP Technologies: Perspectives and Challenges; *P. Cauvet* – Philips - France

16:00-23:00 SOCIAL EVENT & BANQUET

September 7th, 2006

08:30-09:45 SESSION 7

08:30-09:20 Session 7A: Analog Circuit Design 2

Chair: J. MOUINE – ENIT - Tunisia

- **High Frequency CCII Based Oscillators and Multifunction Filters;** *S. Ben Salem, D. Sellami Masmoudi, M. Fakhfakh, M. Loulou, N. Masmoudi;* LETI Sfax -Tunisia
- **Design of enhanced performances CMOS RF mixers suitable for multi-standards receiver;** *S. Douss, M. Loulou;* LETI Sfax, Tunisia.

08:30-09:45 Session 7B: Simulation and Validation

Chair: K. BESBES - FSM - Tunisia

- **Analysis of Multilayer Microstrip Filter by Wave Concept Iterative Process;** *A. Hajlaoui, M. Glaoui, H. Trabelsi;* Faculté des Sciences de Tunis, Tunisia.
- **A SystemC AMS Model of an I2C Bus Controller;** *M. Alassir, J. Denoulet, O. Romain, P. Garda;* Groupe SYEL, LISIF, France.
- **FPGA Implementation of Programmable Pulse Mode Neural Network with on Chip Learning;** *A. Dammak, M. Krid, D. Sellami Masmoudi, N. Derbel;* ICOS, Sfax Engineering School, Tunisia.

09:45-10:45 BREAK & POSTERS

09:45-10:45 Poster Session 4

- **Hardware/Software Approache for the FPFA Implementation of A Fuzzy Logic Controller;** *M. S. Masmoudi, I. Song, F. Karray, M. Masmoudi, N. Derbel;* METS, Tunisia; University of Waterloo, Canada.
- **Performance of adaptive filter used in CDMA system for Multiple Access Interference Suppressing;** *H. Marouane, A. Ben Abdennabi, A. Kachouri, L. Kamoun;* L.E.T.I, Tunisia.
- **Application of the neural network to the synthesis of linear antenna array's radiance diagram;** *R. Ghayoula, ElA. Hajlaoui, M. Glaoui, A. Gharsallah, T. Korkobi;* Laboratory of Electronics, Faculty of Sciences of Tunis; ICOS, Sfax Engineering School, Tunisia.
- **Implementation of a Neural Network Module for Fourth Generation Mobile Equipements;** *E. Damergi, A. Ben Rabaa, A. Bouallegue;* Laboratory of Communication Systems, National Engineering School of Tunis, Tunisia.
- **Folded Cascode OTA Design for Wide Band Applications;** *H. Daoud, S. Ben Salem, S. Zouari, M. Loulou;* LETI, Tunisia.

- **Theoretical and Numerical modeling of a CMOS micromachined acoustic sensor;** *B. Mezghani, K. Haboura, F. Tounsi, S. Smaoui, S. El-Borgi, S. Choura, M. Masmoudi;* METS, National Engineering School of Tunis; Polytechnic School, Tunisia.

10:45-12:25 SESSION 8

10:45-12:25 Session 8A: Special Session on Emerging devices: simulation of CNTFET-based circuits

Chair: R. LEVEUGLE - TIMA - France

- **CNTFET basics and simulation;** *T. Dang, L. Anghel, R. Leveugle;* TIMA Laboratory – France
- **Design-oriented Compact Models for CNTFETs;** *F. Pregaldiny, C. Lallement, J.-B. Kammerer;* InESS – France
- **Analysis of CNTFET physical compact model;** *C. Maneux, J. Goguet, S. Fregonese, T. Zimmer, H. C. d'Honincthum, S. Galdin-Retailleau;* IXL – France; IEF – CNRS, France.
- **CNTFET-based logic circuit design;** *I. O'Connor, J. Liu, F. Gaffiot;* LEOM – France

10:45-12:25 Session 8B: SoC and NoC Design

Chair: M. MASMOUDI – ENIS - Tunisia

- **Performances comparison between Multilevel hierarchical and Mesh FPGA interconnect;** *Z. Marrakchi, H. Mrabet, H. Mehrez;* ASIM-LIP6, France.
- **Universal Low/Medium Speed I²C-Slave Transceiver: a Detailed VLSI Implementation;** *A. K. Oudjida, A. Liacha, D. Benamrouche, M. Goudjil, R. Tiar, A. Ouchabane ;* Centre de Développement des Technologies Avancée (CDTA), Algeria.
- **Dynamic Routing Algorithm for Avoiding Hot Spots in On-chip Networks;** *A. Sobhani, M. Daneshtalab, M. H. Neishaburi, M. D. Mottaghi, A. Afzali-Kusha, O. Fatemi, Z. Navabi;* Low-Power High-Performance NanoSystems Laboratory; University of Tehran, Iran.
- **An Application Specific NoC Mapping for Optimized Delay;** *W. Zhou Y. Zhang, Z. Mao;* Microelectronics Center Harbin Institute of Technology; Harbin Institute of Technology Shenzhen Graduate School, China.

12:25-14:00 LUNCH

14:00-15:40 SESSION 9

14:00-15:40 Session 9A: Low Power Design and Wireless Systems

Chair: A. GHAZEL – SUPCOM - Tunisia

- **Low Power Digital design using modified GDI method;** *P. Balasubramanian, J. John*; School of Electrical Sciences, Vellore Institute of Technology (Deemed University) India.
- **CMOS Leakage Power at Cell Level ;** *R. Mendoza, A. Ferré, L. Balado, J. Figueras*; Universitat Politècnica de Catalunya, Spain.
- **Design of secure digital communication systems using DCSK chaotic modulation;** *M. A. Ben Farah, A. Kachouri, M. Samet*; LETI, Tunisia.
- **A 863-870-MHz Spread-Spectrum Direct Conversion Receiver Design for Wireless sensor;** *H. Trabelsi, G. Bouzid, Y. Jaballi, L. Bouzid, F. Derbel, M. Masmoudi*; METS, Tunisia; Siemens, Germany.

14:00-15:40 Session 9B: New BIST Techniques

Chair: S. BERNARD – LIRMM - France

- **Automated Bist-Based Diagnostic Solution for SOPC;** *A. Sarvi, J. Fan*; Xilinx, Inc.
- **A Low-Power Oscillation Based LNA BIST Scheme;** *J. Machado da Silva*; INESC Porto, Portugal
- **Accumulator – based compression in Symmetric Transparent RAM BIST;** *I. Voyiatzis*; Technological Educational Institute of Athens, Greece.
- **A Distributed BIST Architecture Enabling Extended Sharing and Debug Capabilities;** *J. Tourki, R. Tourki, L. Vachez, L. Ben Ammar*; Electronic and Micro-Electronic laboratory- Tunisia; ATMEL, France.

15:40-16:00 CLOSING SESSION